Claims

What is claimed is:

1. A method of producing a Direct Current (DC) balanced 6B/8B transmission code from an input data stream that includes one or more six-bit source vectors, the method comprising the steps of:

creating, in accordance with an eight binary digit coded vector set, a given coded vector having eight binary digits for a given six-bit source vector of the one or more six-bit source vectors, wherein each coded vector in the eight binary digit coded vector set is balanced; and

outputting the given coded vector.

2. The method of claim 1, wherein the six-bit source vectors are divided into a plurality of sets of six-bit source vectors for the eight binary digit coded vector set.

3. The method of claim 2, wherein one of the plurality of sets comprises all balanced six-bit source vectors.

4. The method of claim 3, wherein the step of creating further comprises the steps of:

selecting a bit sequence of either one followed by zero or zero followed by one; and

adding the selected bit sequence to a six-bit source vector in accordance with the eight binary digit coded vector set to create the given coded vector.

5. The method of claim 4, wherein a second set of the plurality of sets of six-bit source vectors comprises a third set of ten vectors with negative disparity and a fourth set of ten vectors with a positive disparity, each of the vectors in the fourth set being an exact complement of a corresponding vector in the third set.

6. The method of claim 2, wherein one of the plurality of sets comprises all six-bit source vectors with a disparity of plus two with an exception of a six-bit source vector with a trailing run of four ones.

7. The method of claim 6, wherein the step of creating further comprises the step of adding a two-bit sequence having values of zero and zero to a six-bit source vector in accordance with the eight binary digit coded vector set to create the given coded vector.

8. The method of claim 2, wherein one of the plurality of sets comprises all six-bit source vectors with a disparity of minus two with an exception of a source vector with a trailing run of four zeros.

9. The method of claim 8, wherein the step of creating further comprises the step of adding a two-bit sequence having values of one and one to a six-bit source vector in accordance with the eight binary digit coded vector set to create the given coded vector.

10. The method of claim 2, wherein:

a first set of the plurality of sets comprises all balanced six-bit source vectors;

the step of creating further comprises the steps of:

selecting a two-bit sequence of either one followed by zero or zero followed by one; and

adding the selected two-bit sequence to a six-bit source vector from the first set in accordance with the eight binary digit coded vector set to create the given coded vector; and

a second set of the plurality of sets of six-bit source vectors comprises fourteen six-bit source vectors with a disparity of four or six, two six-bit source vectors with a disparity of two and a trailing run of four, and four control vectors.

11. The method of claim 10, wherein the step of creating further comprises the step of adding another two-bit sequence that comprises complements of the values of the selected two-bit sequence to a six-bit source vector from the second set in accordance with the eight binary digit coded vector set to create the given coded vector.

12. The method of claim 11, wherein the step of creating further comprises the step of complementing one to three bits of 16 six-bit source vectors from the second set in such a way that 16 unique six-bit vectors are generated that are balanced with no leading or trailing run of three.

13. The method of claim 12, wherein the 16 six-bit source vectors comprise eight pairs of six-bit source vectors, each pair comprising a six-bit source vector with positive disparity and a corresponding complemented six-bit source vector with negative disparity, and wherein the step of complementing one to three bits involves complementing identical bit positions in any pair of six-bit source vectors.

14. The method of claim 12, wherein the eight-bit coded vectors created using the first set comprise coded data vectors, the eight-bit coded vectors created using the second set comprise coded data and control vectors, and wherein the step of adding two bits that are complements is performed so that when a control input is activated together with any of four predetermined balanced six-bit source vectors, one of four coded control vectors is generated.

15. The method of claim 14, wherein at least one of the coded control vectors has a trailing run of three.

16. The method of claim 15, wherein the coded control vector with a trailing run of three is followed by a coded data vector with a leading run of three whose values match values of the trailing run of three of the control character to generate a two coded vector synchronizing comma sequence.

17. An encoder for producing a Direct Current (DC) balanced 6B/8B transmission code from an input data stream that includes one or more six-bit source vectors, the encoder adapted:

to create, in accordance with an eight binary digit coded vector set, a given coded vector having eight binary digits for a given six-bit source vector of the one or more six-bit source vectors, wherein each coded vector in the eight binary digit coded vector set is balanced; and

to output the given coded vector.

18. A semiconductor comprising at least one encoder for producing a Direct Current (DC) balanced 6B/8B transmission code from an input data stream that includes one or more six-bit source vectors, the at least one encoder adapted:

to create, in accordance with an eight binary digit coded vector set, a given coded vector having eight binary digits for a given six-bit source vector of the one or more six-bit source vectors, wherein each coded vector in the eight binary digit coded vector set is balanced; and

to output the given coded vector.

19. A method of decoding a Direct Current (DC) balanced 6B/8B transmission code from an input data stream that includes one or more eight-bit coded vectors, the method comprising the steps of:

creating, in accordance with an eight binary digit coded vector set, a given uncoded vector having six binary digits for a given eight-bit coded vector of the one or more eight-bit coded vectors, wherein each coded vector in the eight binary digit coded vector set is balanced; and

outputting the given uncoded vector.

20. The method of claim 19, wherein each eight-bit coded vector has two coding binary digits and six uncoded binary digits, the six uncoded binary digits corresponding to a six-bit source vector of a plurality of six-bit source vectors, and wherein the plurality of six-bit

source vectors are divided into a plurality of sets of six-bit source vectors for the eight binary digit coded vector set, wherein each eight-bit coded vector corresponds to one of the six-bit source vectors.

21. The method of claim 20, wherein:

a first of the plurality of sets comprises all balanced six-bit source vectors;

a second of the sets comprises all six-bit source vectors with a disparity of plus two with an exception of a six-bit source vector with a trailing run of four ones;

a third of the sets comprises all six-bit source vectors with a disparity of minus two with an exception of a source vector with a trailing run of four zeros; and

a fourth of the sets comprises fourteen six-bit source vectors with a disparity of four or six, two six-bit source vectors with a disparity of two and a trailing run of four, and four control vectors.

22. The method of step 21, wherein the step of creating further comprises the step of not changing the six uncoded binary digits for all eight-bit coded vectors corresponding to the first, second and third sets.

23. The method of claim 21, wherein the first set has coding binary digits of 10 or 01, the second set has coding binary digits of two zeros, the third set has coding binary digits of 11, and the fourth set has coding binary digits of the inverse of the coding binary digits corresponding to the first set.

24. The method of 23, wherein, when the given eight-bit coded vector corresponds to the fourth set, the step of creating further comprises the steps of:

when the six uncoded binary digits of the given coded vector comprise one of 16 unique six-bit uncoded vectors, complementing one to three bits of the six uncoded binary digits in accordance with the eight binary digit coded vector set;

when the six uncoded binary digits of the given coded vector comprise one of four unique control vectors, asserting a control signal; and

for other coded vectors corresponding to the fourth set, dropping the two coding binary digits for the coded vectors.

25. The method of claim 19, further comprising the step of declaring the given eight-bit coded vector as valid if the given eight-bit coded vector is balanced with a run of no more than three at the leading end of the given eight-bit coded vector or of no more than three at the trailing end of the given eight-bit coded vector.

26. The method of claim 21, further comprising the step of activating a control signal when a control vector is created in the step of creating.

27. The method of claim 19, wherein the step of creating further comprises the step of:

determining, by using two binary digits of the given eight-bit coded vector, whether certain binary digits of the given eight-bit coded vector require changing,

wherein the eight binary digit coded vector set is designed so that only one of four possible combinations of the two binary digits indicate that binary digits of an eight-bit coded vector require changing.

28. A decoder for decoding a Direct Current (DC) balanced 6B/8B transmission code from an input data stream that includes one or more eight-bit coded vectors, the decoder adapted:

to create, in accordance with an eight binary digit coded vector set, a given uncoded vector having six binary digits for a given eight-bit coded vector of the one or more eight-bit coded vectors, wherein each coded vector in the eight binary digit coded vector set is balanced; and

to output the given uncoded vector.

29. A semiconductor comprising at least one decoder for decoding a Direct Current (DC) balanced 6B/8B transmission code from an input data stream that includes one or more eight-bit coded vectors, the at least one decoder adapted:

to create, in accordance with an eight binary digit coded vector set, a given uncoded vector having six binary digits for a given eight-bit coded vector of the one or more eight-bit coded vectors, wherein each coded vector in the eight binary digit coded vector set is balanced; and

to output the given uncoded vector.